THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 13

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte JENS HORSTMANN
and YOON KIM

_____

Appeal No. 1997-3241
Application 08/442,726

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ON BRIEF

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Before HAIRSTON, FLEMING, and BARRY, **Administrative Patent Judges**.

FLEMING, **Administrative Patent Judge**.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 15, 16 and 17. Claims 1-14 have been canceled.

The invention relates to a Translation Lookaside Buffer (TLB) which utilizes a Least-Recently-Used (LRU) algorithm for determining the replacement of data. On page 8 of the

specification, Appellants identify that each storage location (referred to as a slice) includes a ripple counter which contains a value indicative of the time the data in the slice was used relative to the data within the buffer's other slices. Each of these counters is connected to a comparator which compares the value of the counter with a reference value. As described in greater detail on page 16 of Appellants' specification, the comparison is performed using a technique whereby the lower order bits of the counter are compared to the reference value at the same time the ripple counter is incrementing the higher order bits. This technique reduces the overall time required to update the counter and compare the count to the reference value. Additionally, use of the ripple counter, in lieu of a synchronous counter, reduces the circuit elements needed in the TLB.

Independent claim 15 is illustrative of the invention.

15. A method, comprising:

initiating an incrementing of a ripple counter of an LRU portion of a translation lookaside buffer by clocking a low order bit of said ripple counter; and

comparing an output value of said low order bit of said ripple counter with a low order bit value of a ripple counter

broadcast value on a reference bus when said ripple counter is still incrementing due to said clocking.

The Examiner relies upon the following references:

Moyer	4,002,926	Jan. 11, 1977
Miu et al. (Miu)	4,783,735	Nov. 8, 1988
Okamoto et al. (Okamoto)	4,910,668	Mar. 20, 1990

The following rejections are appealed.

Claims 15, 16 and 17 are rejected under 35 U.S.C. § 102 as being anticipated by Miu.

Claim 17 is rejected under 35 U.S.C. § 103 as being unpatentable over Okamoto and Moyer.

Rather than reiterate the arguments of Appellants and the Examiner, reference is made to the brief and the answer for the respective details thereof.

Opinion

We will not sustain the rejection of claims 15, 16, and 17 under 35 U.S.C. § 102, nor will we sustain the rejection of claim 17 under 35 U.S.C. § 103.

First, we consider the rejection of claims 15, 16 and 17 under 35 U.S.C. § 102 as being anticipated by Miu. Anticipation is established only when a single prior art reference discloses, expressly or under the principles of inherency, each and every element of a claimed invention as well as disclosing structure which is capable of performing the recited functional limitations. ***RCA Corp. v. Applied Digital Data Sys. Inc***., 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir. 1984), ***cert. dismissed***, 468 U.S. 1228 (1984); ***W. L. Gore & Assoc., Inc. v. Garlock Inc***., 721 F.2d 1540, 1554, 220 USPQ 303, 313 (Fed. Cir. 1983), ***cert. denied***, 469 U.S. 851 (1984).

The Examiner asserts on page 3 of the answer that "[t]he claimed 'ripple counter' corresponds to the initialize counter 10-50, MUX 10-52, MUX 10-54, replacement level generator 10-6 and cache control circuits 10-4 shown in figures 1-3." Further, the Examiner asserts that the comparing is performed by comparators 10-602, 10-622. On page 4 of the answer, the Examiner contends that Miu teaches in column 4, lines 39-53,

that the comparison is performed while the counter increments.

On page 7 of the brief, Appellants assert that Miu does not teach the use of a ripple counter. Further, Appellants assert that Miu does not teach that the comparison is performed while the counter is incrementing.

As pointed out by our reviewing court, we must first determine the scope of the claim. "[T]he name of the game is the claim" ***In re Hiniker Co.*** 150 F.3d 1362, 1369, 47 USPQ2d 1523, 1529 (Fed. Cir. 1998). Claims will be given their broadest reasonable interpretation consistent with the specification, limitations appearing in the specification are not to be read

into the claims. ***In re Etter***, 756 F.2d 852, 858, 225 USPQ 1, 5 (Fed. Cir. 1985). In analyzing the scope of the claim, office personnel must rely on the Appellants' disclosure to properly determine the meaning of terms used in the claims. ***Markman v. Westview Instruments***, 52 F.3d 967, 980, 34 USPQ2d 1321, 1330 (Fed. Cir.)(***in banc***), ***aff'd***, U.S., 116 S. Ct. 1384 (1996). An applicant is entitled to be his or her own lexicographer, and in many instances will provide an explicit definition for certain terms used in the claims. Where an explicit definition is provided by the applicant for a term, that definition will control interpretation of the term as it is used in the claim. Office personnel should determine if the original disclosure provides a definition consistent with any assertions made by applicant. See, e.g., ***In re Paulsen***, 30 F.3d 1475, 1480, 31 USPQ2d 1671, 1674 (Fed. Cir. 1994)(inventor may define specific terms used to describe invention, but must do so "with reasonable clarity, deliberateness, and precision" and, if done, must "'set out his uncommon definition in some manner within the patent

disclosure' so as to give one of ordinary skill in the art notice

of the change" in meaning)(quoting ***Intellicall, Inc. v. Phonometrics, Inc.***, 952 F.2d 1384, 1387-88, 21 USPQ2d 1383, 1386 (Fed. Cir. 1992)).

We find that the scope of independent claims 15 and 17 includes using a ripple counter and comparing the output value of the counter's lower order bit to a reference value while the ripple counter is still incrementing. These limitations are shown in claim 15, "initiating an incrementing of a ripple counter . . . by clocking a low order bit of said ripple counter" and "comparing an output value of said low order bit of said ripple counter with a low order bit value of a ripple counter broadcast value on a reference bus when said ripple counter is still incrementing due to said clocking." These limitations are also shown in claim 17, "incrementing the ripple counter" and "during the step of incrementing, after the first one of the plurality of binary bits is updated and before the last one of the plurality of binary bits is updated, comparing the updated first one of the plurality of binary bits with a corresponding bit broadcast on a reference bus."

The term “ripple counter” is not defined in the specification. However, figure 11 of the specification provides the schematics of a ripple counter. On page 4 of the brief, Appellants describe a ripple counter as a counter where the least significant bit is updated first, then the next significant bit, and so on until all the bits of the counter have been updated to reflect the incrementation. Thus, it takes several clock cycles until all bits of the counter reflect the incremented value. This description is consistent with the operation of the counter and comparator described on page 16 of Appellants' specification, which identifies that the comparator uses the low order bits of the counter while the higher order bits are incrementing. Further, this definition of a ripple counter is consistent with the known meaning in the art as is evidenced by Moyer who discloses in column 1, lines 28-51 and column 4, line 36 to column 5 line 11, that a ripple counter is one where the first bit is clocked then the output of the first bit clocks the next bit, and so on. Thus, we find that the limitation of a ripple counter should be given its normal meaning in the art, a counter in which the least significant bit is incremented

first and then the next bit and so on until all bits of the counter have been updated to reflect the count.

We next consider the limitation "comparing when said ripple counter is still incrementing." On page 8 of the brief, Appellants assert that this limitation means that there is an overlapping of the incrementing and comparing steps. On page 16 of the specification, Appellants identify that "the pipelining technique allows the lower order bits of each LRU counter to be compared to the value on the reference bus at the same time when the higher order bits of the LRU counter are still incrementing," where the LRU counter is a ripple counter. Accordingly, we find that the limitation of "comparing when said ripple counter is still incrementing," means that a comparison is made between the lower order bits of the counter and a reference value while the count is propagating through the higher order bits, i.e., comparison of lower order bits is made before the higher order bits of the counter have been updated to reflect the count.

Having determined the scope of the claims, we next turn to the art applied in the rejection. Miu discloses using a counter to initialize a memory. As described in Miu, column

4, lines 39-53, counter 10-50 is used to provide a value to the first register and to each of a plurality of comparators. Each of these comparators is associated with a register. The comparator compares the counter's value with the previous register's value to determine if the previous register's value is to be loaded into the comparator's register. The result of this operation is that the initialization counter is counting through its entire range, each register is sequentially assigned a value. We find that Miu does not disclose that counter 10-50 is a ripple counter. Further, we find that the comparison taught by Miu is not performed on the lower order bits while the count is propagating through the higher order bits. Accordingly, we will not sustain the rejection of claims 15, 16 and 17 under 35 U.S.C. § 102.

Next, we will consider the rejection of claim 17 under 35 U.S.C. § 103 as being unpatentable over Okamoto and Moyer. The Examiner has not set forth a ***prima facie case***. It is the burden of the Examiner to establish why one having ordinary skill in the art would have been led to the claimed invention by the express teachings or suggestions found in the prior

art, or by the implications contained in such teachings or suggestions. ***In re Sernaker***, 702 F.2d 989, 995, 217 USPQ 1, 6 (Fed. Cir. 1983). "Additionally, when determining obviousness, the claimed invention should be considered as a whole; there is no legally recognizable 'heart' of the invention." ***Para-Ordance Mfg. V. SGS Importers Int'l Inc.***, 73 F.3d 1085, 1087, 37 USPQ2d 1237, 1239 (Fed. Cir. 1995), ***cert. denied***, 519 U.S. 822 (1996)(***citing W.L. Gore & Assoc., Inc. v. Garlock Inc***., 721 F.2d 1540, 1548, 220

USPQ 303, 309 (Fed. Cir. 1983), ***cert. denied***, 469 U.S. 851 (1984)).

The Examiner asserts on page 6 of the answer that Okamoto teaches LRU using a counter (item 24) in a translation lookaside buffer. The Examiner further states that Okamoto makes use of a comparator (item 70), but that Okamoto does not make use of a ripple counter. The Examiner relies upon Moyer to teach a ripple counter. Finally, on page 7 of the answer, the Examiner asserts that Okamoto teaches in column 4, line 62 through column 5, line 4 and column 5, line 47 through column 6, line 42, that the comparison is made while the counter is incrementing.

Appellants argue on page 9 of the brief that the combination of Okamoto and Moyer does not teach the claimed relationship of overlapping the comparison process and incrementation of the ripple counter.

As identified above, we find that the scope of claim 17 includes that there is a comparison of the lower order bits of the ripple counter with a reference value before the higher order bits of the counter are updated to reflect the count.

We find that neither Okamoto nor Moyer teaches or suggests that a comparison step should be performed on the lower order bits of a ripple counter before the higher order bits are updated to reflect the incrementation. Accordingly, we will not sustain the rejection of claim 17 based upon 35 U.S.C. § 103.

In view of the foregoing, we reverse the Examiner's rejection of claims 15, 16 and 17 under 35 U.S.C. § 102 as being unpatentable over Miu. Further, we reverse the rejection of claim 17 under 35 U.S.C. § 103 as being unpatentable over Okamoto and Moyer.

REVERSED

KENNETH W. HAIRSTON)
Administrative Patent Judge)
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)
) BOARD OF PATENT
MICHAEL R. FLEMING)
Administrative Patent Judge) APPEALS AND
)

) INTERFERENCES
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LANCE LEONARD BARRY)
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